B. Tech.
(SEM. II) THEORY EXAMINATION 2011-12
ELECTRONICS ENGINEERING

Time : 3 Hours
Total Marks : 100

Note : All sections are compulsory.

SECTION—A

1. All questions are compulsory. All questions carry equal marks :

\[(10 \times 2 = 20)\]

(a) Describe the difference between donor and acceptor impurities.

(b) What is voltage multiplier ?

(c) What is the ripple factor for full wave rectifier ?

(d) Derive the relation between \( \alpha \) and \( \beta \) for BJT.

(e) Write down the stability factors for BJT amplifier.

(f) What is pinch-off condition in FET ?

(g) Draw the circuit of voltage summer using Op-amp and write the expression.

(h) What are MAXTERM and MINTERM ?

(i) What are Lissajous figures ?

(j) What are the necessary blocks in the multimeter for measuring AC voltage ?
2. Attempt any three parts of the following. All questions carry equal marks: \((10 \times 3 = 30)\)

(a) Draw and explain the Center-tapped transformer full-wave rectifier.

A full wave bridge rectifier use \(R_L = 2 \, \text{k}\Omega\), each diode is to have forward resistance \(R_f = 2 \, \Omega\) and \(R_r = \infty\). A sinusoidal voltage having peak amplitude of 20 V is applied. Find out:

(i) Peak, dc and rms values of load current;
(ii) dc and rms output voltages;
(iii) dc output power;
(iv) ac input power;
(v) Efficiency.

(b) Derive the complete hybrid equivalent model of BJT in common emitter configuration. For the network of figure 1:

(i) Determine \(I_{CQ}\) and \(V_{CEQ}\)
(ii) Find \(V_{B^2}, V_{C^2}, V_{E^2}, V_{BC}\)

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**Figure 1**
(c) Why is the input impedance to a JFET so high? Also justify the sentence JFET as a voltage controlled resistor.

Given \( I_{DSS} = 6 \text{ mA} \) and \( V_p = -4.5 \text{ V} \)

(i) Determine \( I_D \) at \( V_{GS} = -2 \) and \(-3.6 \text{ V}. \)

(ii) Determine \( V_{GS} \) at \( I_D = 3 \) and \( 5.5 \text{ mA}. \)

(d) Explain the working of Digital multimeter and write down the general specifications. What are the different types of D'VMs? Explain one of them.

SECTION—C

Note: All questions are compulsory. All questions carry equal marks.

10 \( \times 5 = 50 \)

3. Attempt any two parts of the following. All questions carry equal marks:

(a) Sketch \( i_R \) and \( v_o \) for the network of Figure 2 for the input shown.

(b) 

![Diagram](image)

Figure 2

EC201/PUR-40806(Re)
(b) Justify the sentence 'the zener diodes are used as voltage regulators and limiters'.
Design the network of Figure 3 to maintain \( V_L \) at 12 V for a load variation \( (I_L) \) from 0 mA to 200 mA. That is, determine \( R_S \) and \( V_Z \).

![Figure 3](image)

(c) For the network of Figure 4:
(i) Calculate \( 5\tau \)
(ii) Compare \( 5\tau \) to half the period of the applied signal
(iii) Sketch \( v_o \).

![Figure 4](image)
4. Attempt any two parts of the following. All questions carry equal marks:

(a) What do you mean by Limits of operation in BJT amplifier? Also draw the input and output characteristics of a BJT in the common base configuration.

(b) Draw and solve the Voltage divider bias circuit of BJT by any one of the method.

(c) For the circuit shown in Figure 5:
   (i) Determine $I_C$
   (ii) Prove stabilization factor $S(I_{CO}) = \frac{\beta + 1}{1 + \beta \frac{R_E}{R_E + R_B}}$

![Figure 5](image_url)
5. Attempt any two parts of the following. All questions carry equal marks:

(a) Draw and solve the self-bias configuration of JFET.
(b) Explain the construction and working of n-chann depletion type MOSFETs.
(c) The network of Figure 6 is not operating properly. What is the specific cause of its failure?

![Figure 6](image)

6. Attempt any two parts of the following. All questions carry equal marks:

(a) (i) Convert the following:
\[(389)_{10} = ( \_ )_8 \quad (FB27)_{16} = ( \_ )_8 \quad (11001101)_{2} = ( \_ )_{16}\]

(ii) Convert the following into POS format:
\[y(A, B, C, D) = (A + B + C) \cdot (A + D)\]

EEC201/PUR-40806(Re)
(b) (i) Design a circuit using only NOR gates for Boolean expression:

\[ Y = ABC' + BCD' + CD. \]

(ii) Subtract by using r’s complement method where r is the base of the number:

\( (3762)_r \) and \( (2664)_r \) \( (11.0101)_r \) and \( (11.100)_r \)

(c) State the DeMorgan’s theorems.

Minimize the following using K-map technique:

\[ F(A, B, C, D) = AB'C' + A'BC + A'B'CD + ABCD + \Sigma d(1, 5) \]

7. Attempt any two parts of the following. All questions carry equal marks:

(a) What are the applications of a CRO? How do you measure frequency of an unknown signal using Lissajous figure in CRO.

(b) Draw and derive the expression for differentiator with op-amp. What is the range of the voltage gain adjustment in the circuit of Figure 7.

Figure 7

\[ \begin{array}{c}
\text{500 k}\Omega \\
\text{10 k}\Omega \\
\text{10 k}\Omega \\
\end{array} \]
(c) Write short notes on the following:

(i) Transition and diffusion capacitance of p-n junction diode

(ii) Construction of a CRT.