**RAJ KUMAR GOEL INSTITUTE OF TECHNOLOGY & MANAGEMENT, GZB**

**1st Sessional Examination 2017-18 ( Odd Semester)**

**Roll No.:**  **Subject Name: CA**

**Year/Branch**: **3rd/CSE Subject Code:** **NCS-505**

**Max Time: 1Hours 30 Minute Max Marks: 50**

**SECTION-A**

**Q.1 Attempt all parts.Each part carry equal marks.Write answers in brief. (2x5=10)**

(a) Design 4 bit adder subtractor circuit using block diagram.

(b) Discuss the elements of bus design.

(c) Examine the address field of an indexed addressing mode instruction to make it the same as a register indirect mode instruction?

(d) Draw the block diagram for the hardware that implements:

 x+yz : R1<-R2 + R3

(e) Starting from initial values R=10101110 determine the sequence of binary values in R after logical shift left,followed by circular shift right,followed by logical shift right and circular shift left.

**SECTION-B**

**Note: Attempt any five questions from this section. (5x5=25)**

**Q.2** Analyse the hardware implementation and algorithm for addition and subtraction of numbers in sign magnitude numbers.

**Q.3** A two-word instruction is stored in memory at an address designated by symbol W. the address field of the instruction (stored at W+1) is designated by the symbol Y. the operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is:

a. Direct

b. Indirect

c. Relative

d. Indexed

**Q.4** Elaborate the Instruction Types with five examples of each type.

**Q.5** A bus –Organization CPU has 64-bit registers with 32 bit in each, an ALU,destination decoder and shifter.

i. How many multiplexers are there in the A bus, and determine the size of multiplexer.

ii. Mention the selection inputs needed for MUX A and MUX B.

iii. Identify the number of inputs and outputs in the decoder?

iv. Calculate the number of inputs and outputs are in ALU for data, including input and output carries?

v. Formulate a control word for the system assuming that ALU has 63 operations and shifter has 8 operations.

**Q.6** Inspect the working of ALU with a logic diagram of ALU that perform AND, OR logic operations and ADD, SUB arithmetic operations.

**Q.7** Discuss serial and parallel bus arbitration methods with proper diagram?

**Q.8** Design an arithmetic circuit with one selection variable **S** and two **n**-bit data inputs **A** and **B**. The circuit generates the following four arithmetic operations in conjunction with the input carry **Cin**. Draw the logic diagram for the first two stages :

**S Cin=0 Cin=1**

**0 D=A+B D=A+1**

 **1 D=A-1 D=A+B'+1**

**Q.9** Prepare the algorithm of multiplication for signed bit numbers with flow chart.

**SECTION-C**

**Note: Attempt any two questions from this section. (7.5x2=15)**

**Q.10** Conclude the multiplication process using Booth’s algorithm when the following numbers are multiplied.

(-9) \* (+21)

**Q.11** Write a program to evaluate the arithmetic statement

X= [A\*B+E\*(C+D)] / (G\*H+K)

 using three, one and zero address machine.

**Q.12** Discuss direct, indirect, relative, register direct and register indirect addressing mode. Also distinguish between implied and immediate addressing mode with suitable instructions.